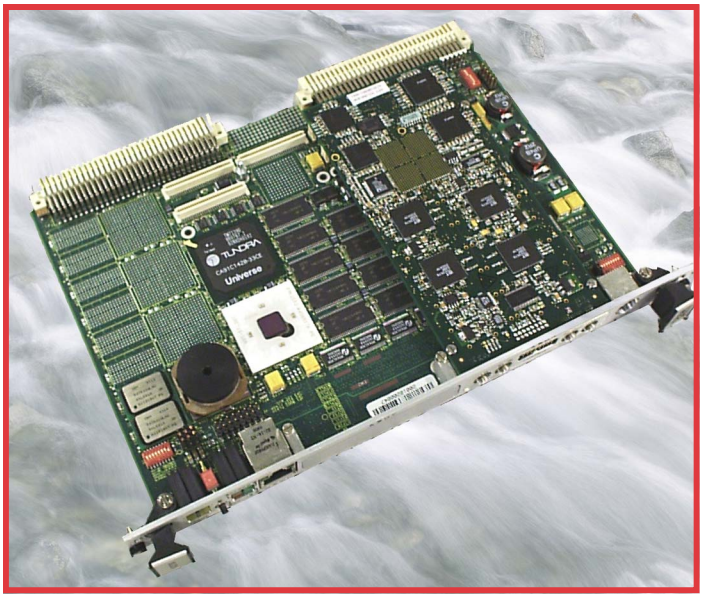
Red River

Interceptor VME/RACE

Model 108



- *Single/Dual/Quad PowerPC Architecture*
- *VME64 and RACE / RACE++ Interfaces*
- *70 MHz Analog IF (Baseband Optional)*
- *40 MHz Analog IF Bandwidth*
- *8 MHz Maximum Signal Bandwidth*
- *Up to 16 Channels*
- *Up to 90 dB Linear Dynamic Range*
- *Front Panel Control for Synchronization*
- *VxWorks and Linux RTOS Support*
- *VSIPL Signal Processing Library*
- *Includes Waveformer Configuration Tool*

PowerPC Software Defined Radio Receiver

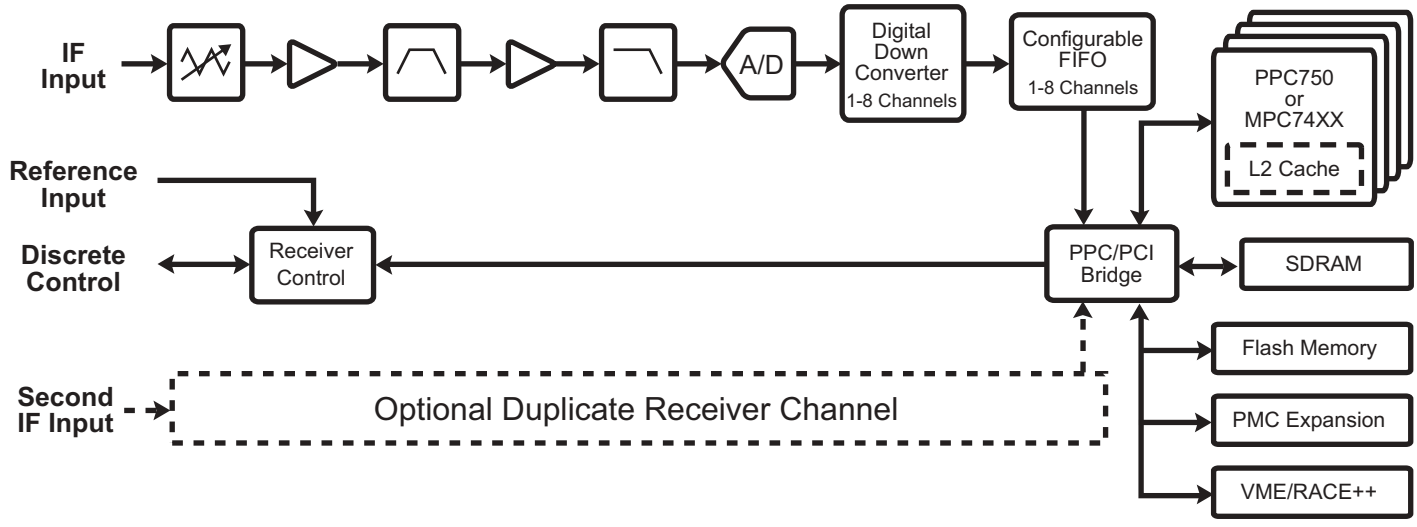
Interceptor provides a complete software defined radio receiver solution in a single-slot VME format. The unique polychannel architecture combines the flexibility, performance, and precision of advanced digital downconverter chips with a modern analog IF front-end to address both narrowband and wideband applications. The dedicated receiver hardware is supplemented with a multi-processor general purpose computer to tackle the most demanding signal processing algorithms. Software development is supported by industry standard real-time operating systems and the Vector Signal and Image Processing Library optimized for AltiVec processors.

The receiver accepts an analog IF input through an SMB connector located on the front panel. The signal is routed through a digitally controlled attenuator and buffer amplifier immediately preceding the analog anti-alias filter. A second amplifier stage boosts the signal to match the input range of the A/D converter.

Samples out of the A/D converter are passed to a digital downconverter that can produce from one to eight independent output channels. The maximum signal bandwidth available in each channel increases as the number of channels is reduced. Each channel tunes to a signal of interest and performs amplitude adjustment based on gain control settings.

The complex data samples produced by the downconverter are stored in a configurable FIFO. The FIFO organization can be matched to the number of active output channels. The depth of each FIFO is also variable, allowing higher sample rate channels to obtain more memory.

DMA transfers from the receiver can be initiated either autonomously by the receiver or under direct control of the host. Each FIFO is assigned a programmable threshold that signals either the local controller or the host for service.



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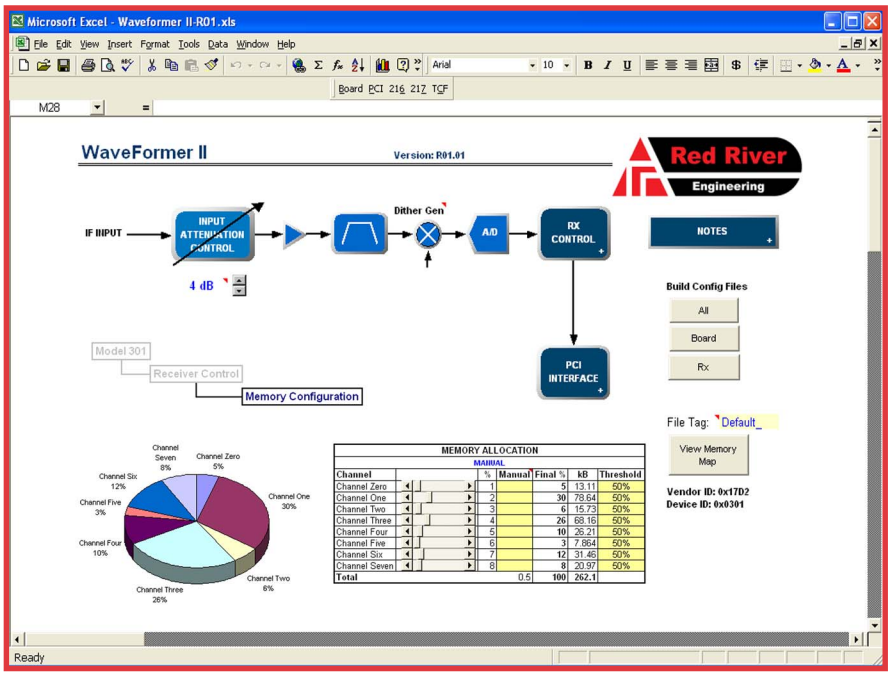

The Waveformer configuration tool simplifies receiver programming.

The *Interceptor* provides software access to all control registers, including the receiver input attenuator level, FIFO memory allocation by channel, downconverter (ISL5216) configuration space, local command/status, and receiver data flow control. The receiver interface includes an interrupt to alert the processor of an error condition or data service request.

Interceptor programming is simplified by the *Waveformer* configuration tool that automates the process of computing register values based on the desired performance characteristics of the receiver. The user enters configuration information through a series of menu-driven spreadsheets that accept input based on available register options. The spreadsheets also perform error checking to eliminate configuration conflicts and graphically display key performance parameters in simple block diagrams and frequency response plots. The configuration tool generates a file containing the complete memory map that can be easily uploaded to the receiver.

Typical Applications

- Signal Intelligence (SIGINT) Collection
- Beamforming / TDOA (Smart Antenna, E911)
- Multi-Mode Software Defined Radio Receiver
- Multi-Channel Narrowband Digital Receiver
- Single Channel Wideband Digital Receiver

Specification Summary

Receiver

70 MHz IF Center Frequency
20 MHz IF Bandwidth
-15 dBm Input Power (Full Scale)
+5 dBm 3rd Order Intercept Point
40 dB Analog Gain Control
14-bit, 93.3 MSPS A/D Converter
Intersil ISL5216 Downconverter
1-8 Independent Output Channels
8 MHz Maximum Signal Bandwidth
(Single Channel Operation)
2 MHz Maximum Signal Bandwidth
(Eight Channel Operation)
256 kbyte Configurable Data FIFO
Digital Automatic Gain Control
90 dB Linear Dynamic Range (30kHz)

Processor

1, 2 or 4 PowerPC Processors
466 MHz PPC750 (1 MB Cache)
500 MHz MPC7410 (2 MB Cache)
2 MB Boot Flash / 32 MB Flash Pool
128 - 512 MB SDRAM with ECC

Board

Single-Slot 6U Eurocard Format
VME64 and RACE/RACE++ I/F
Industry Standard PMC Site
SMB Coaxial Analog I/O
10 MHz 3 ppm Local Reference
5 to 25 MHz Reference Input

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