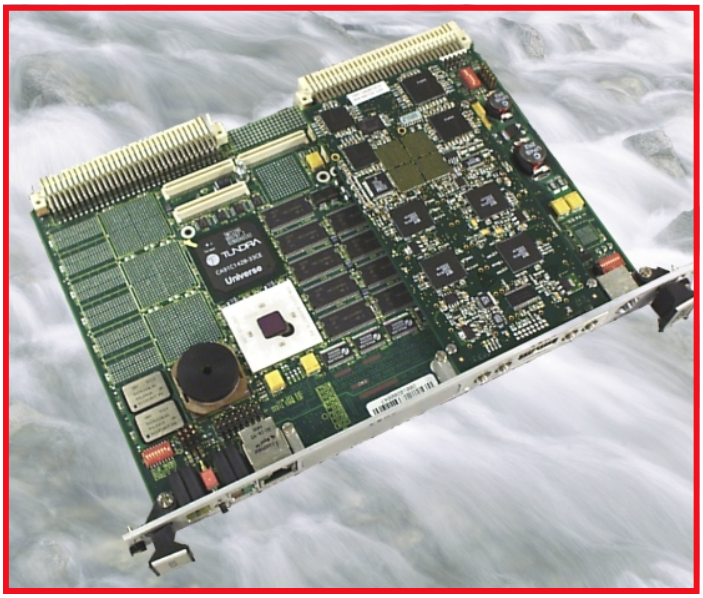
Red River

SoftRadio VME/RACE

Model 103/104/105



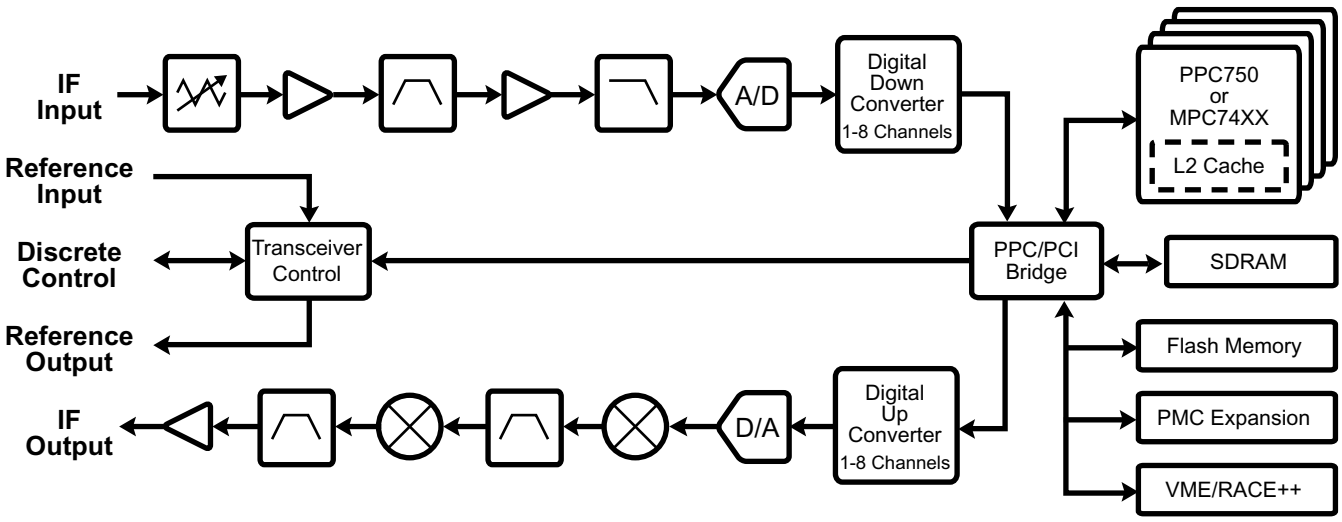
- *Single/Dual/Quad PowerPC Architecture*
- *VME64 and RACE / RACE++ Interfaces*
- *70 MHz Analog IF (Baseband Optional)*
- *20 MHz Analog Receive Bandwidth*
- *40 MHz Analog Transmit Bandwidth*
- *5 MHz Maximum Signal Bandwidth*
- *Up to 8 Transmit and Receive Channels*
- *Front Panel Control for Synchronization*
- *VxWorks and Linux RTOS Support*
- *VSIPL Signal Processing Library*
- *Includes Waveformer Configuration Tool*

PowerPC Software Defined Radio

The *SoftRadio* provides a complete software defined radio solution in a single-slot VME format. The unique polychannel architecture combines the flexibility, performance, and precision of advanced digital transceiver chips with a modern analog IF front-end to address a broad range of both narrowband and wideband applications. The dedicated transceiver hardware is supplemented with a multi-processor general purpose computer to tackle the most demanding signal processing algorithms. Software development is supported by industry standard real-time operating systems and the Vector Signal and Image Processing Library optimized for AltiVec processors.

The *SoftRadio* receiver accepts an analog IF input through an SMB connector located on the front panel. The signal is routed through a digitally controlled attenuator and buffer amplifier immediately preceding the analog anti-alias filter. A second amplifier stage boosts the signal to match the input range of the A/D converter. The second IF produced by the A/D converter is passed to a digital downconverter that can be configured for one to eight independent output channels. Each channel tunes to a signal of interest and performs amplitude adjustment based on gain control settings. The complex data samples produced by the downconverter are stored in a FIFO that is accessed through DMA transfers initiated by the processor or transceiver.

The *SoftRadio* transmitter data flow begins with the DMA transfer of samples from the processor to the transmit FIFO. The samples are rate buffered out of the FIFO to match the clock frequency at the input of the digital upconverter. The upconverter filters and interpolates from one to eight independent channels to produce a single wideband digital IF at the D/A converter input. The resulting analog signal is passed through two conversion stages to produce a final IF that is supplied through an SMB coaxial connector located on the front panel.



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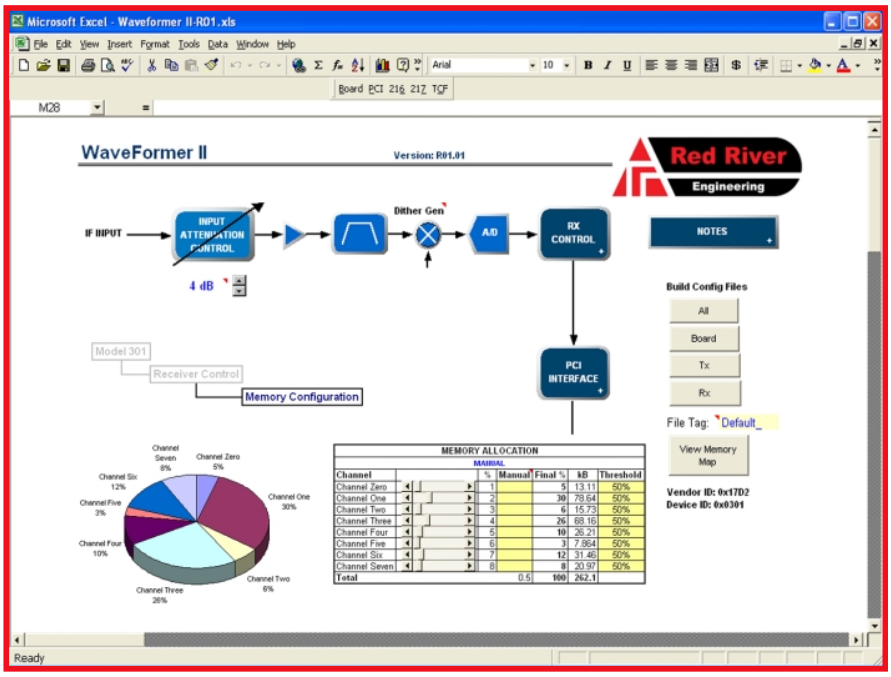

The Waveformer configuration tool simplifies radio programming.

The *SoftRadio* provides software access to all transceiver control registers, including the receiver input attenuator level, FIFO memory allocation by channel, programmable downconverter configuration space, programmable upconverter configuration space, transceiver command/status, and transceiver data flow control. The transceiver interface includes an interrupt to alert the processor of an error condition or data service request.

SoftRadio programming is simplified by the *Waveformer* configuration tool that automates the process of computing register values based on the desired performance characteristics of the transceiver. The user enters configuration information through a series of menu-driven spreadsheets that accept input based on available register options. The spreadsheets also perform error checking to eliminate configuration conflicts and graphically display key performance parameters in simple block diagrams and frequency response plots. The configuration tool generates a file containing the complete memory map that can be easily uploaded to the transceiver.

Typical Applications

- Multi-Mode Base Stations (1G, 2G, 2.5G, 3G)
- Beamforming / TDOA (Smart Antenna, E911)
- Military Communications (AM, FM, FSK, PSK, DAMA)
- Multi-Mode Software Radio
- Multi-Mode Wireless Local Loop
- Satellite Communications

Specification Summary

Receiver

70 MHz IF Input (20 MHz BW)
-15 dBm Input Power (Full Scale)
+5 dBm 3rd Order Intercept Point
40 dB Analog Gain Control
14-bit, 56 MSPS A/D Converter
Intersil HSP50214 or ISL5216 PDC
1-8 Independent Output Channels
256 kbyte Configurable Data FIFO
5 MHz Maximum Signal Bandwidth
Digital Automatic Gain Control
90 dB Linear Dynamic Range (30kHz)

Transmitter

1-8 Independent Input Channels
256 kbyte Configurable Data FIFO
Intersil HSP50215 or ISL5217 PUC
10 MSPS Max Complex Input
14-bit, 75 MSPS D/A Converter
5 MHz Maximum Signal Bandwidth
70 MHz IF Output (40 MHz BW)
-15 dBm Output Power (Full Scale)
+5 dBm 3rd Order Intercept Point
70 dB Spur-Free Dynamic Range

Processor

1, 2 or 4 PowerPC Processors
466 MHz PPC750 (1 MB Cache)
500 MHz MPC7410 (2 MB Cache)
2 MB Boot Flash / 32 MB Flash Pool
128 - 512 MB SDRAM with ECC

Board

Single-Slot 6U Eurocard Format
VME64 and RACE/RACE++ I/F
Industry Standard PMC Site
SMB Coaxial Analog I/O
10 MHz 3 ppm Local Reference
5 to 25 MHz Reference Input

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