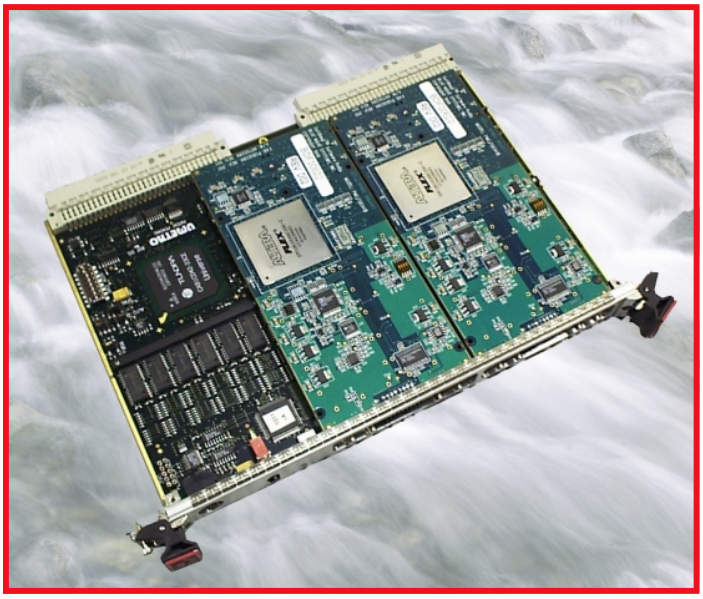
Red River

# WaveWalker VME/RACE

## Model 101/102



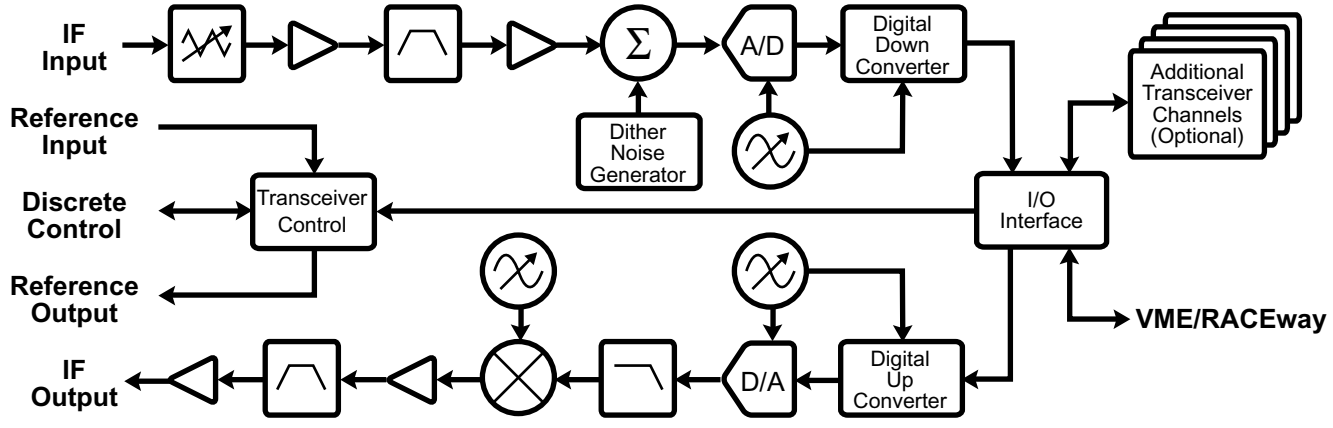
- *Industry Standard VME Form Factor*
- *Software Defined Radio Building Block*
- *70 MHz IF / 12.5 MHz Analog Bandwidth*
- *1.25 MHz Digital Receiver Bandwidth*
- *1.25 MHz Digital Transmitter Bandwidth*
- *Up to 90 dB Linear Dynamic Range*
- *-20 dBm Max Input / +5 dBm Input TOI*
- *Software Programmable Sample Rates*
- *Simple Memory-Mapped Host Interface*
- *Front Panel Control for Synchronization*
- *Includes Waveformer Configuration Tool*

## 1-5 Channel Programmable Digital Transceiver

*WaveWalker VME/RACE* adds a high performance software defined radio capability to any 6U VME chassis. The product combines the flexibility, performance, and precision of advanced digital transceiver chips with a modern analog IF front-end to provide a complete end-to-end solution. The industry standard VME/RACEway interface offers compatibility to a wide range of host processors and target platforms. The Model 101 provides either one or two full duplex channels in a single slot. The model 102 is a dual slot card that can be configured for up to five channels. Both cards feature independent receive and transmit datapaths that share a common interface to the VMEbus or RACEway crossbar interconnect.

The receiver accepts an analog IF input through an SMB connector located on the front panel. The signal is routed through a digitally controlled attenuator and buffer amplifier immediately preceding the analog anti-alias filter. A second amplifier stage boosts the signal to match the input range of the A/D converter. The second IF produced by the A/D converter is passed to a digital downconverter that tunes to the signal of interest and performs amplitude adjustment based on gain control settings. The complex data samples produced by the downconverter are stored in a FIFO for extraction by the host.

The transmitter data flow begins at the host interface with the transfer of data samples from the processor to a FIFO located on the module. The samples are rate buffered out of the FIFO to match the clock frequency at the input of the digital upconverter. The upconverter performs a digital filter operation followed by a frequency translation to establish a first IF compatible with the input to the D/A converter. The output of the D/A converter passes through an analog interpolation filter and mixer for upconversion to the final IF. The output signal is supplied through an SMB coaxial connector on the front panel after a final stage of signal conditioning.



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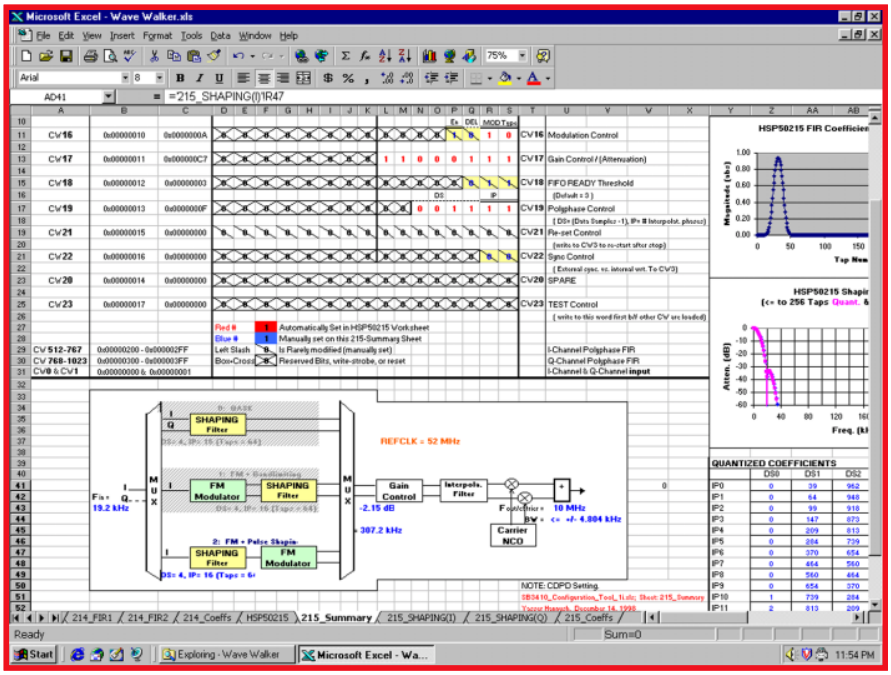


***The Waveformer configuration tool simplifies transceiver programming.***

Each *WaveWalker VME/RACE* channel occupies 16k of memory space offset from a base address register. The host processor has direct access to all control registers, including the receiver input attenuator level, dither noise power level, receiver sample rate, downconverter (HSP50214) configuration space, transmitter sample rate, upconverter (HSP50215) configuration space, local command/status, and transceiver data flow control. The bus interface includes an interrupt to alert the host of an error condition or data service request.

*WaveWalker VME/RACE* programming is simplified by the *Waveformer* configuration tool that automates the process of computing register values based on the desired performance characteristics of the transceiver. The user enters configuration information through a series of guided spreadsheets that describe the purpose of each control register, setting options, and default values. The spreadsheets also perform error checking to eliminate configuration conflicts and graphically display key performance parameters in architecture block diagrams and frequency response plots. The configuration tool generates a file containing the complete memory map that can be uploaded from the host.

## Typical Applications

- Multi-Mode Base Stations (GSM, AMPS, IS54, IS95)
- Beamforming / TDOA (Smart Antenna, E911)
- Military Communications (AM, FM, FSK, PSK, DAMA)
- Multi-Mode Wireless Local Loop
- Software Defined Radio
- Satellite Communications

## Specification Summary

### Receiver

70 MHz Analog IF Input
12.5 MHz Analog Input Bandwidth
-20 dBm Input Power (Full Scale)
+5 dBm 3rd Order Intercept Point
40 dB Variable Analog Gain Control
12-bit, 53 to 60 MSPS A/D
Harris HSP50214 Downconverter
1.25 MHz Max Digital Bandwidth
Digital Automatic Gain Control
90 dB Linear Dynamic Range (30kHz)

### Transmitter

5.5 MSPS Max Complex Input
Harris HSP50215 Upconverter
3.25 MHz Max Digital Bandwidth
14-bit, 45 to 52 MSPS D/A
70 MHz Analog IF Output
12.5 MHz Analog Output Bandwidth
-15 dBm Output Power (Full Scale)
+25 dBm 3rd Order Intercept Point
80 dB Spur-Free Dynamic Range

### Board

6U Compliant Physical
VME64/RACEway Interface
SMB Coaxial Analog I/O
12.80 MHz 3 ppm Local Reference
5 to 25 MHz Reference Input

### Options

Baseband Analog I/O
PMC, PCI, CPCI Solutions Available
Customization Available by Request

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