PERFORMANCE TECHNOLOGIES

innovative IP communications

PICMG 2.16, CompactPCI/PSB

Packet Switching Backplane

Applied Computing Conference

05-16-2001

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PICMG 2.16 Chairman

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What are we going to cover?

- ✓ What is PICMG 2.16?
- ✓ Why is it being developed?
- ✓ What are its objectives?
- ✓ How is it implemented?
- ✓ Some typical applications.
- ✓ Summarize all of the above.
- ✓ Answer your questions!!!

What is PICMG 2.16?

- Assigned as PICMG 2.16 on September 14th 2000.
- Over 96 individuals, from over 75 companies have joined.
- Originator of 2.16 is Performance Technologies Inc.
- Co-sponsors are Hybricon and Natural Microsystems.
- 5 spec revisions to date, latest being 0.5.0 as of 4/2001.
- First PICMG 2.16 meeting held in Boston on 11/09/2000.
- Fast Track Schedule, sub-committee meets every month.
- PICMG 2.16 Chairman is John Peters (PTI).
- Secretaries are Joe Muczynski(PTI) and Joe Kennedy(Intel).
- Specification ratification is presently targeted for 8/2001.

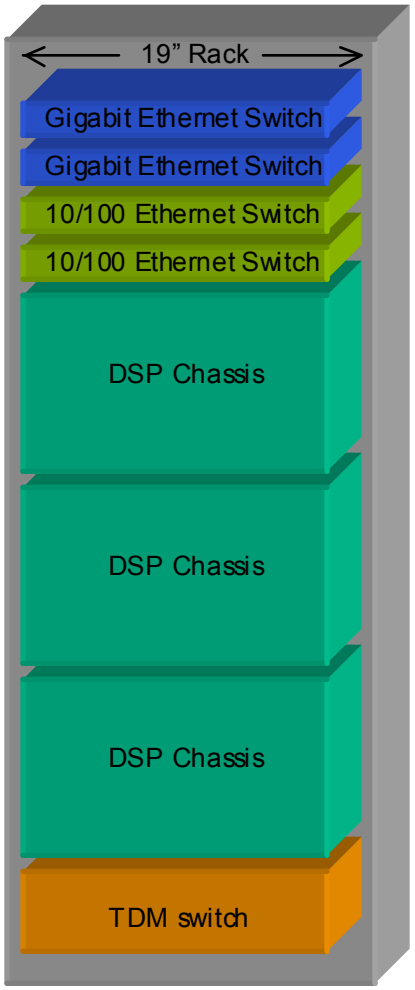
What is PICMG 2.16?

"CompactPCI/PSB is an extension to the PICMG 2.x family of specifications that overlays a packet based switching architecture based on Ethernet, on top of CompactPCI, to create an Embedded System Area Network (ESAN)."

What is PICMG 2.16?

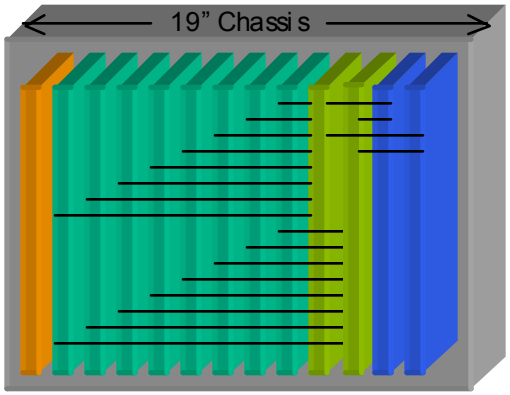
"An Embedded System Area Network (ESAN) is all about "pushing" today's network technology into the chassis and leveraging the ubiquity of Ethernet/IP."

What is PICMG 2.16?



Convert cables to PCB traces!

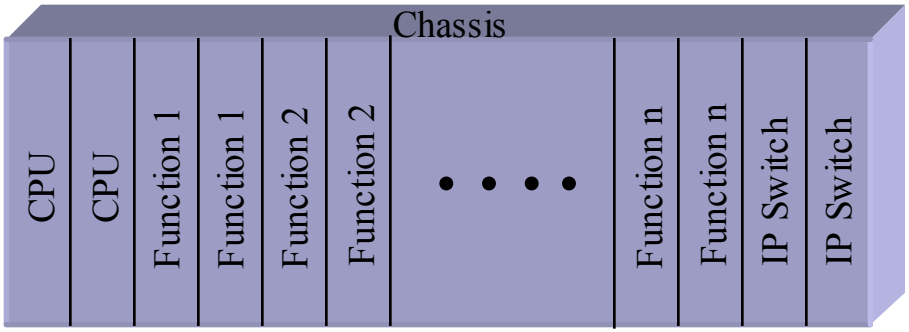
Treat "blades" as "systems"!



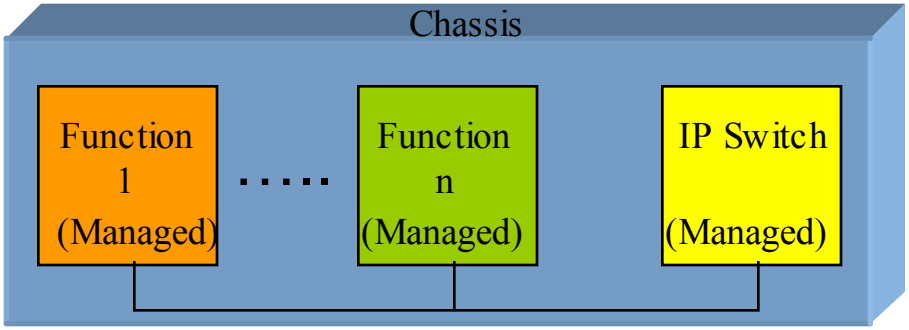
Embedded System Area Network

What is PICMG 2.16?

Backplane Perspective



Today – Centralized management/single parallel shared bus

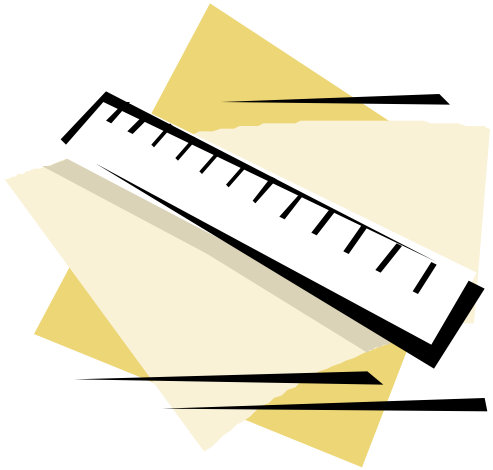


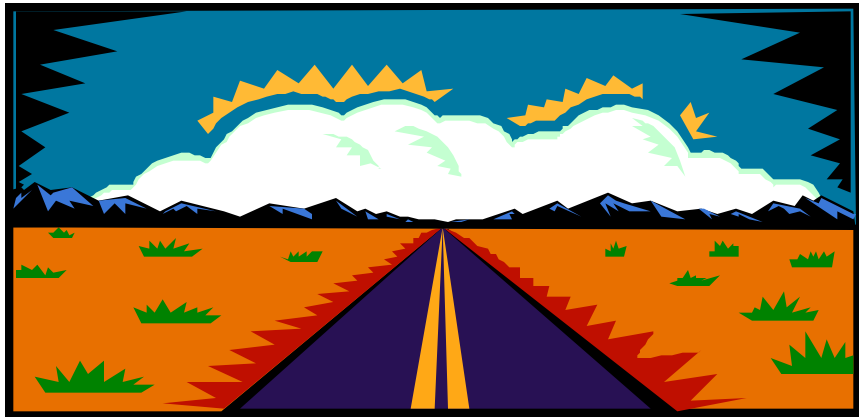
PICMG 2.16 – De-centralized management/redundant P2P switched serial bus

Why is it being developed?

It's about Networking @

the "1st inch" vs. "the last mile"

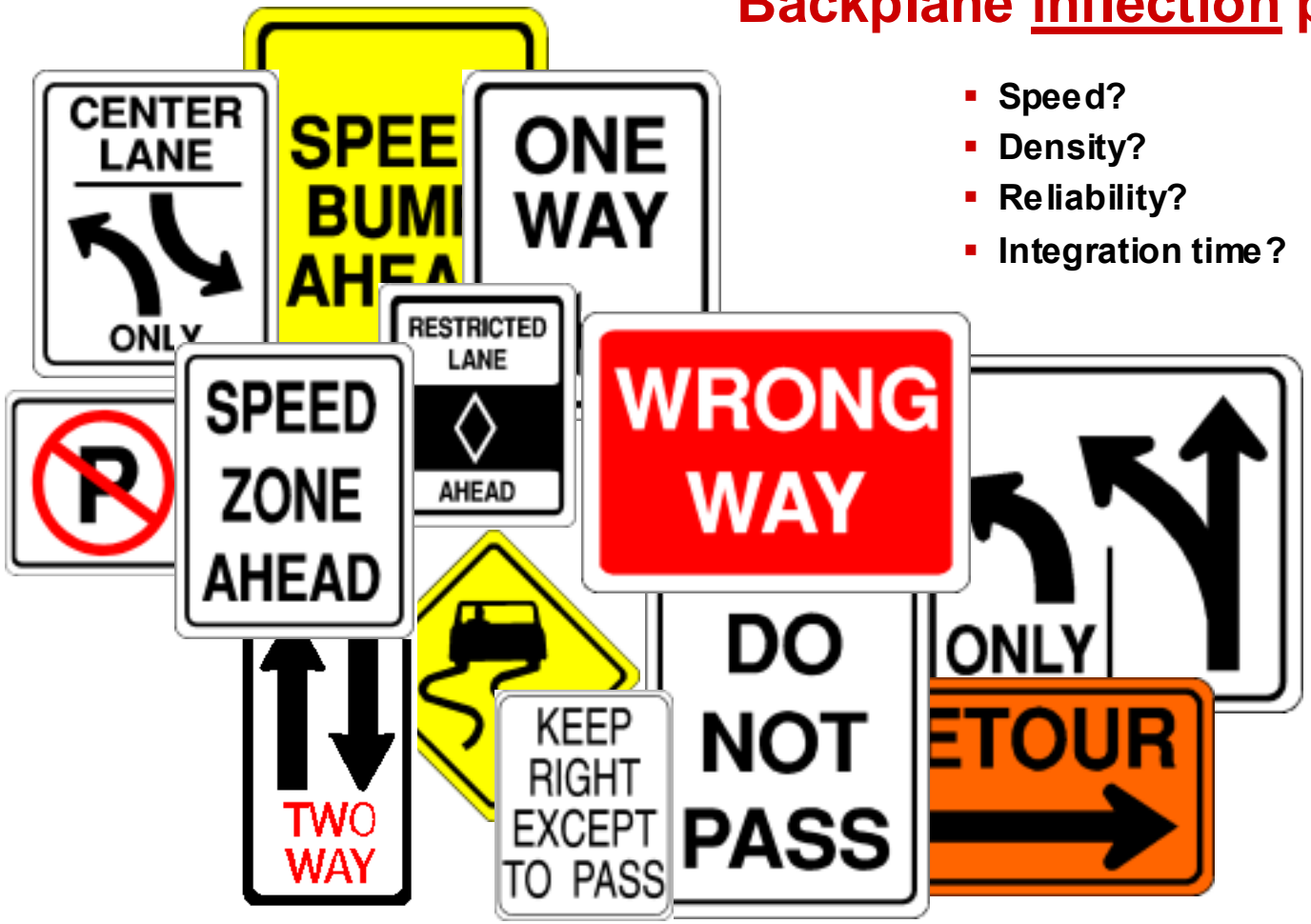




Why is it being developed?

Backplane inflection point?

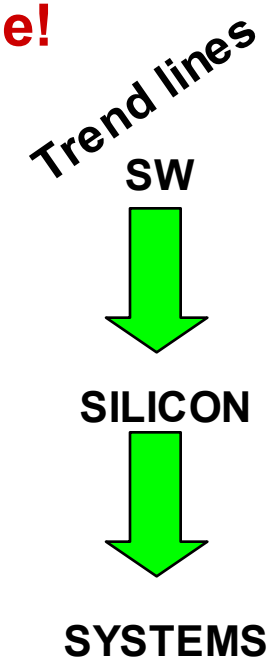
- Speed?
- Density?
- Reliability?
- Integration time?



Why is it being developed?

Industry need to reduce system integration time!

Improve TTM



1st Processor technology promoted compiler based software languages

absolute code performance/density traded off for SW design speed/control/management **>>>(TTM)**

Then Process technology promoted logic synthesis and HDL

absolute gate count/performance traded off for silicon design speed/control/management **>>>(TTM)**

Now! Packet Backplanes will promote integration at the network/transport layers

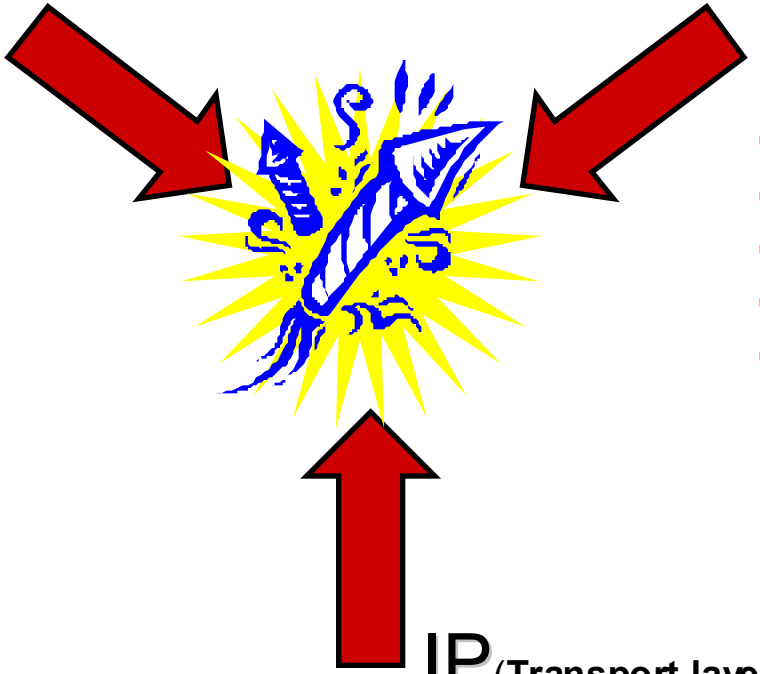
traditional memory mapped I/O traded for improved system integration speed/control/management/reliability **>>>(TTM)**

Why is it being developed?

PICMG 2.16 is a *revolutionary* solution using *evolutionary* technology.

CompactPCI

- Standards based
- Mechanicals
- Power Dist
- Hot Swap



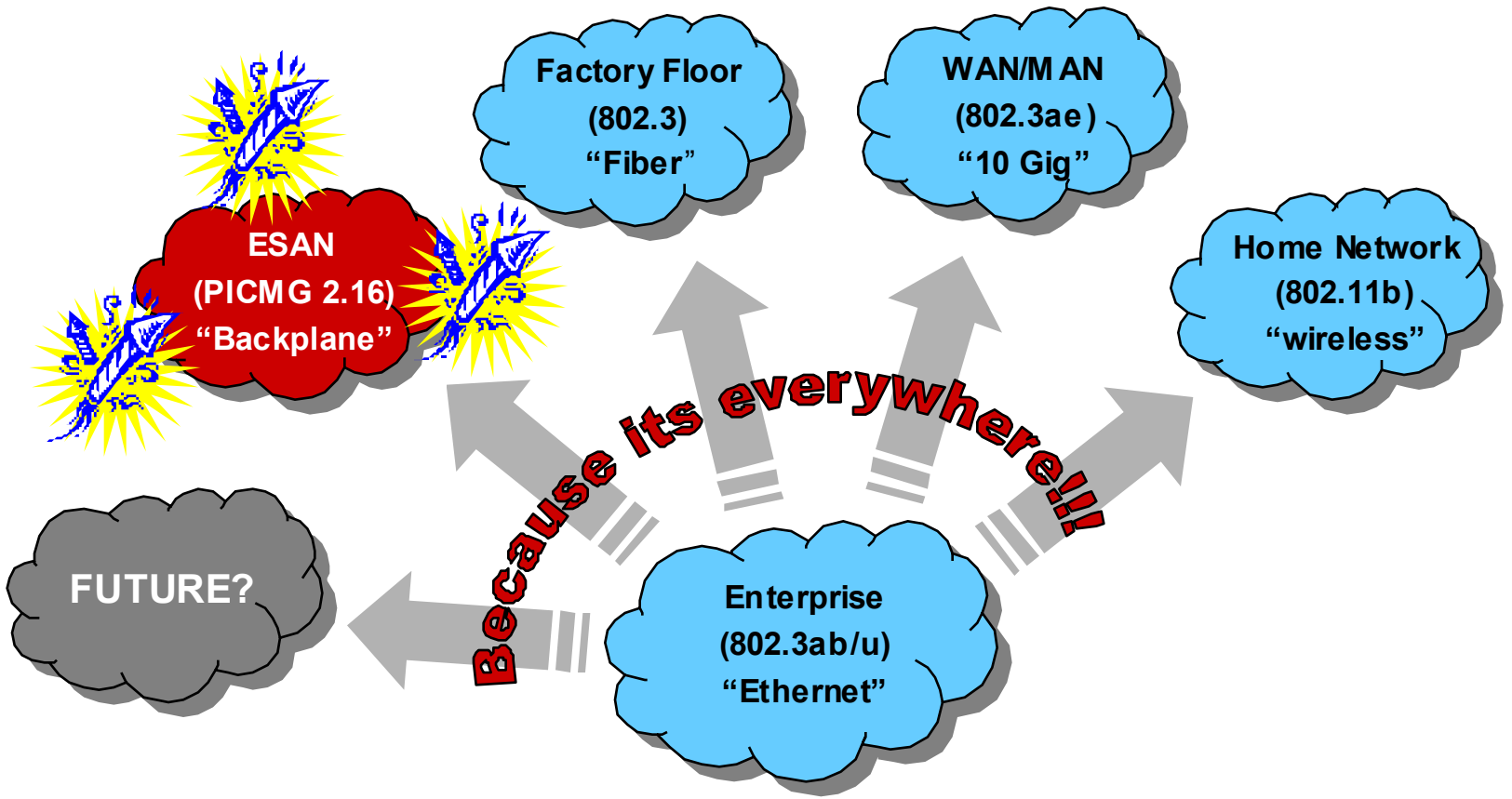
Ethernet

- Standards based
- Media Access Controller ICs
- Physical Interface ICs
- Switching Fabric ICs
- Protocols

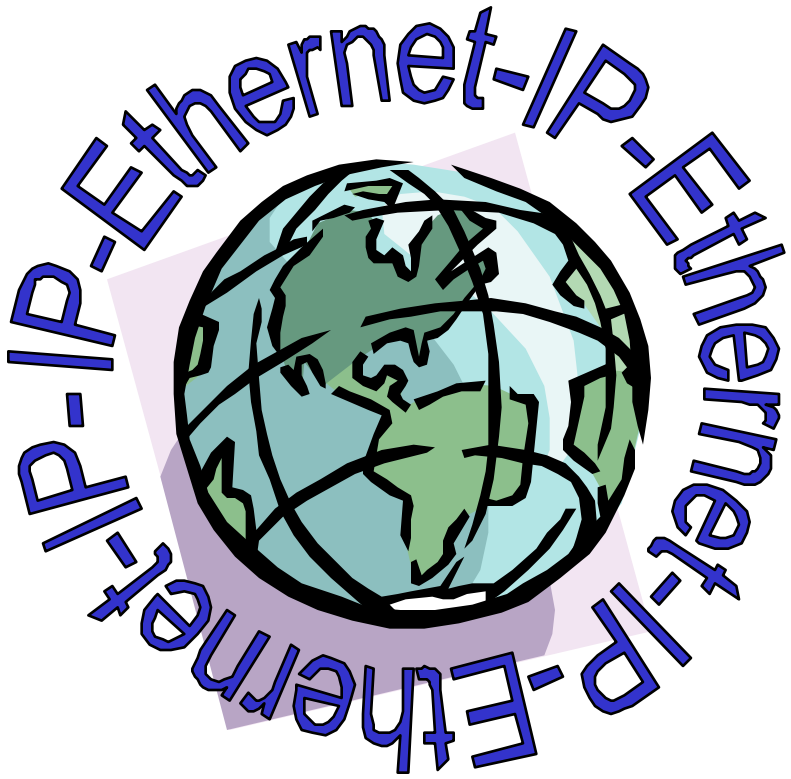
IP (Transport layers, Applications)

Why is it being developed?

Why Ethernet?



Why is it being developed?



Internet and Ethernet are becoming synonymous

- Absolute dominance of IP-based service
- 95% world wide data travels on Ethernet
- 85% of installed networks are Ethernet

Why is it being developed?

Resistance is futile…… ☺

What are its objectives?

1) Reduce integration time
2) Increase system reliability
3) Improve density/performance
4) Enhance existing CompactPCI
5) Provide architectural scalability
6) Leverage ubiquity of IP/Ethernet

What are its objectives?

Performance:

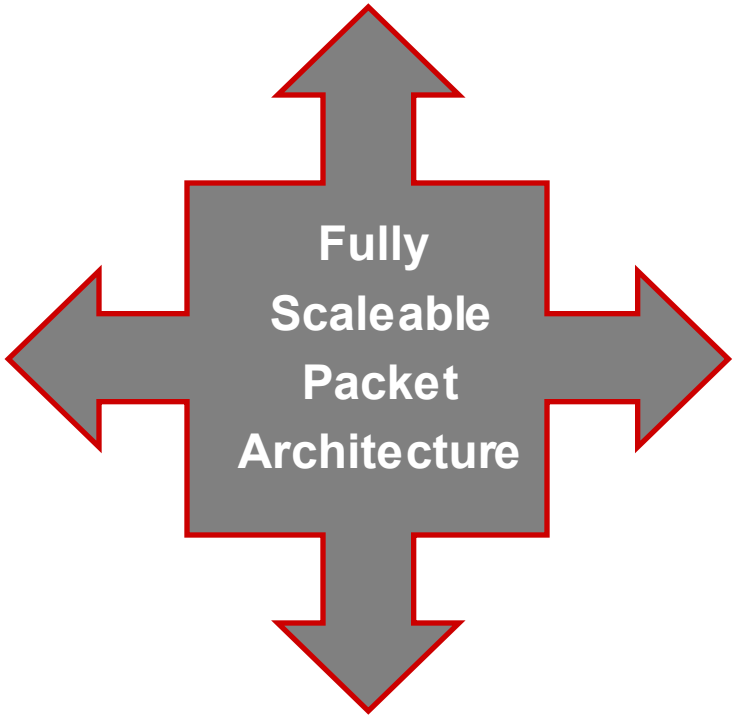
10 to 4000Mbits/slot

Cost $$$:

10Mbit – 1Gigabit

One or two fabrics

Commodity silicon



Reliability:

dual fabrics

SPF @ slot level

Density:

1-21 slots+

"virtual" backplanes

What are its objectives?

2.16 Features:

- ✓ Standards based architecture (I.e. Ethernet, commodity silicon, IP etc.)
- ✓ Scalable system performance: Up to 48 Gigabits/chassis (1 chassis).
- ✓ Scalable reliability: 1 or 2 fully independent fabrics (HA capable).
- ✓ Scalable cost: single fabric/10Mbit to dual fabric/gigabit.
- ✓ Scalable bit rate/slot (10-1000Mbit) using Ethernet "Auto Negotiation".
- ✓ "Fine" granularity P2P architecture, single point of failure (SPF) = 1 slot.
- ✓ "Virtual backplane" capable allowing for multi-chassis architectures.
- ✓ Single backplane design can support all configurations and options.
- ✓ Concise pinout requires only 16 connections per node slot
- ✓ Inherently hot swappable and HA due to network based architecture.
- ✓ Upgradeable architecture by simple adding/changing fabrics/nodes.

How is it implemented?

Definitions

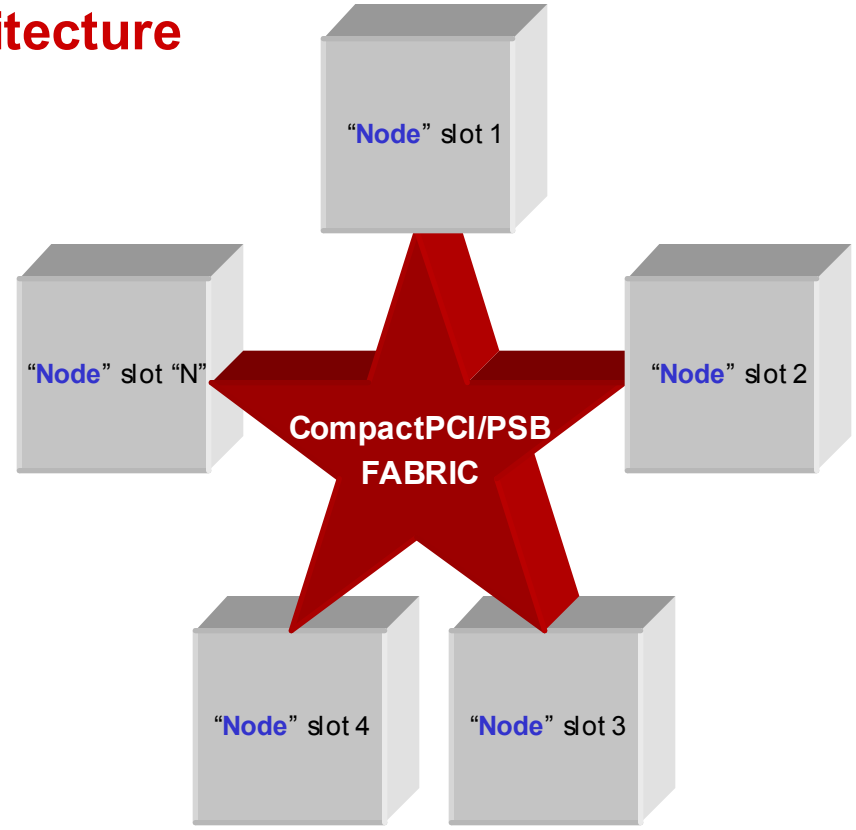
Only <u>two</u> slots types:

1.) **Node**

2.) **Fabric**

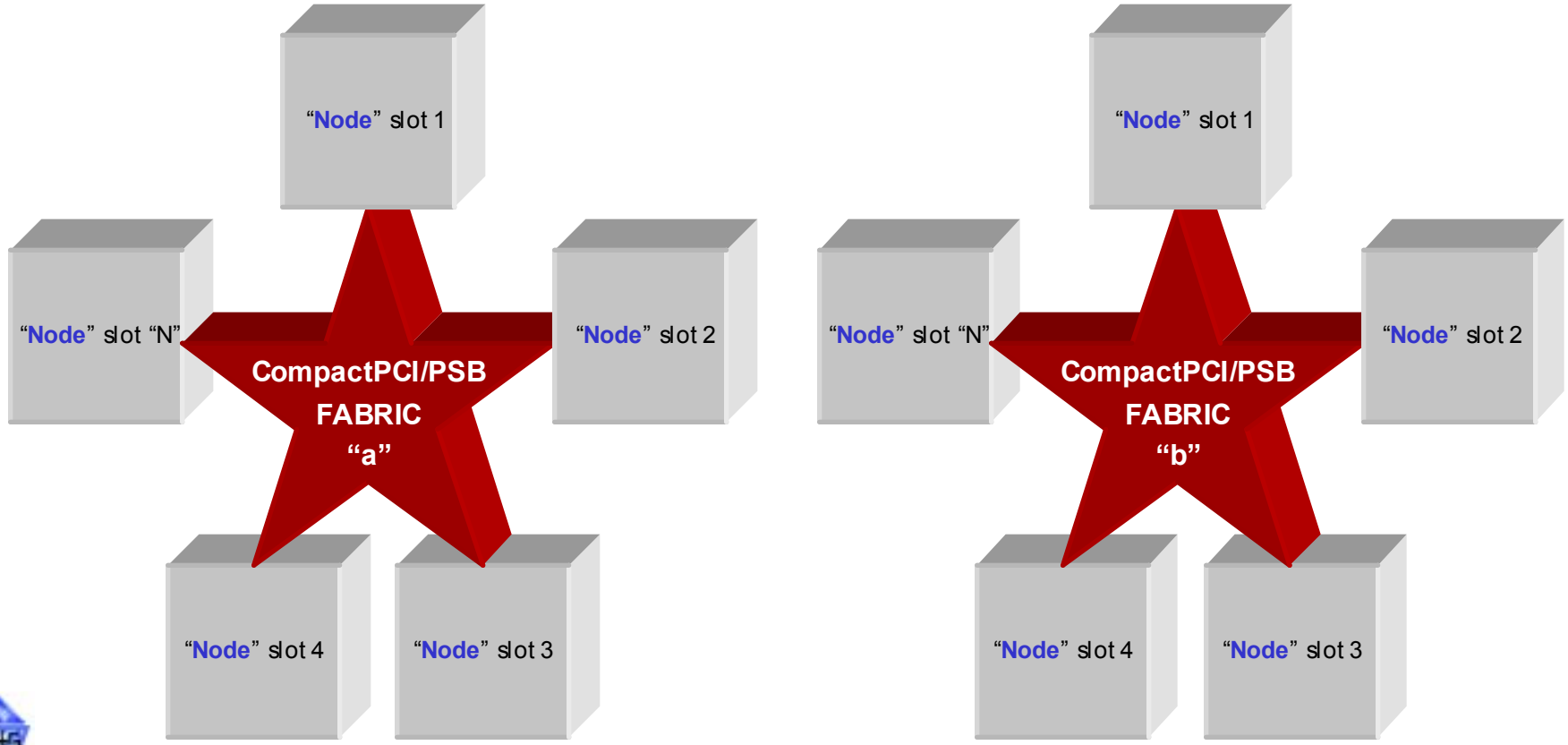
How is it implemented?

Simple “STAR” architecture



How is it implemented?

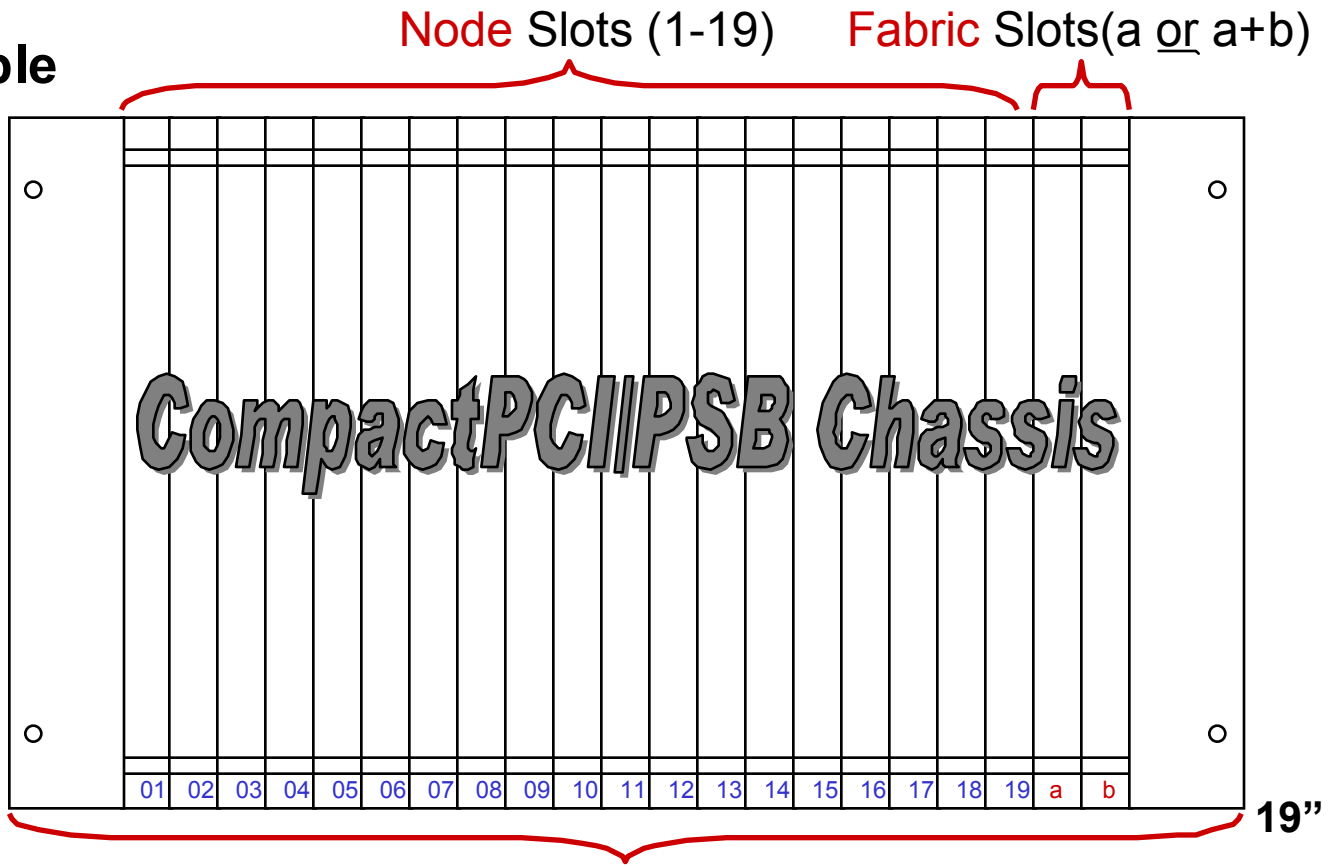
Simple redundant "STAR" architecture



How is it implemented?

Fabric/Node **21 slot CompactPCI/PSB chassis**

chassis example



How is it implemented?

node definition

Nodes slots 1-19 (optionally 1-24)

- Contain PSB node boards connected to one or both PSB fabrics (a or a+b).
- Connections between node slots and fabric slots are via links.
- A node slot may support one link port (fabric a) or two link ports (fabrics a+b).
- Up to 19 node slots may be supported in a CompactPCI/PSB chassis.
- Up to 24 node slots may be supported using the optional “extended” fabric.
- Any node slot may support 1 or 2 link ports (a or a+b) @10/100/1000Mbits.
- Connection to the CompactPCI/PSB fabrics (a+b) is done via 16 J3/P3 pins.
- All Link Port connections to the CompactPCI/PSB fabrics are Hot Swappable.
- Available bandwidth for each node slot can be up to 4Gb/s.

How is it implemented?

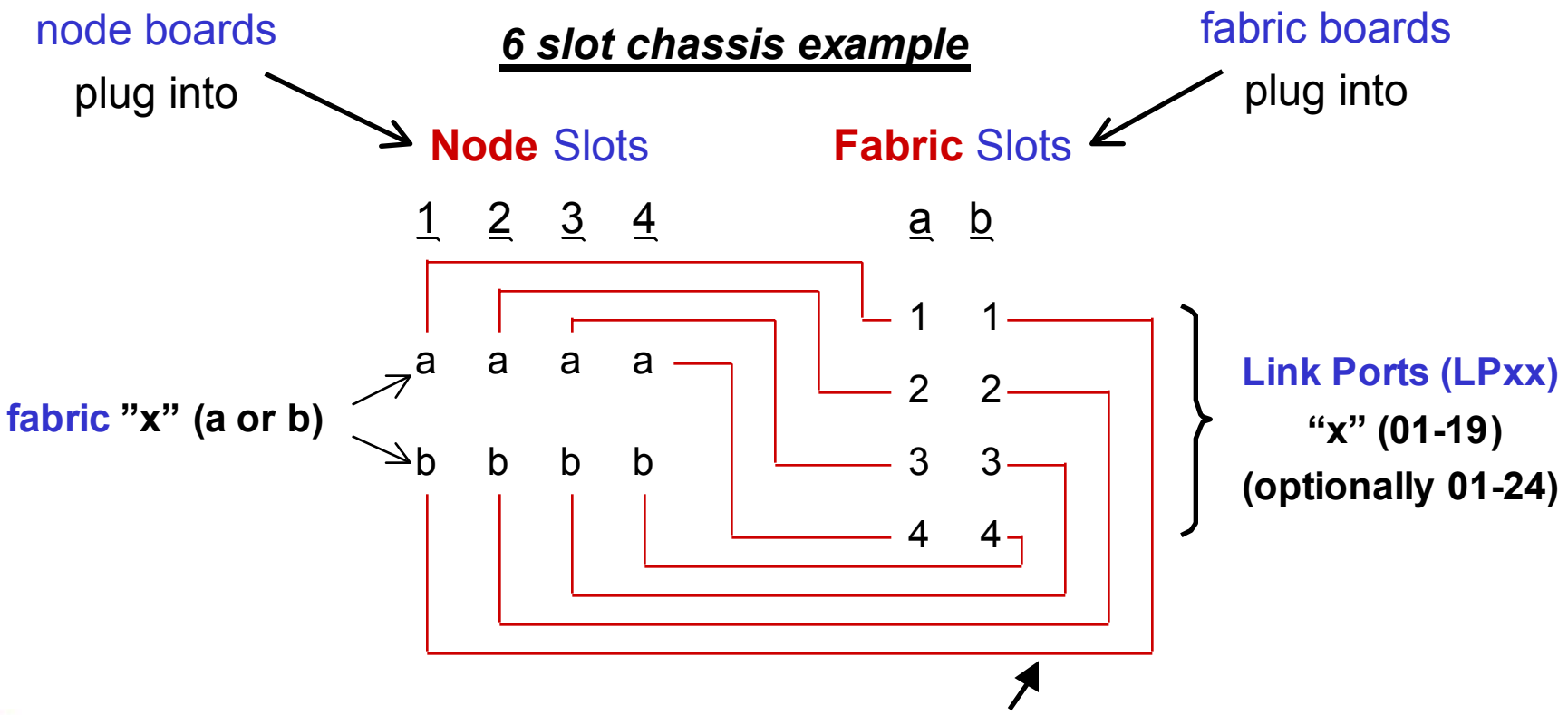
fabric definition

Fabric slots (a or b):

- Contain PSB fabric boards connected to 1 - 24 PSB links. (extended fabric)
- Fabric boards in fabric slots switch packets between multiple node slots.
- Connections between fabric slots and node slots are via links.
- A fabric slot may support between 1 and 24 link ports ea @10/100/1000Mbits.
- Up to 2 fabric slots may be supported in a CompactPCI/PSB backplane.
- Connection to the CompactPCI/PSB fabric(s) is done via 192 P3/P4/P5 pins.
- All fabric slot connections to the CompactPCI/PSB fabric(s) are Hot Swappable.
- Available bandwidth for each fabric slot can be up to 48Gb/s (extended fabric)
- Fabric to Fabric connections are supported via a dedicated link port (f).

How is it implemented?

Node/Fabric slot interconnect example

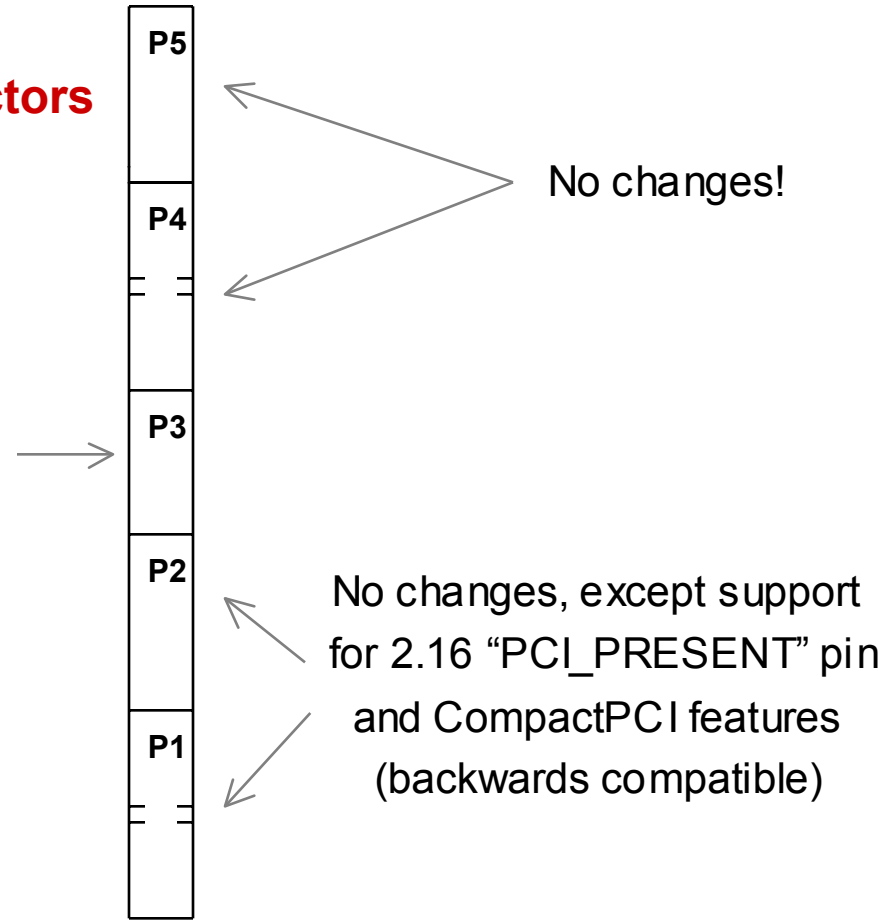


How is it implemented?

PSB Design: node slot connectors

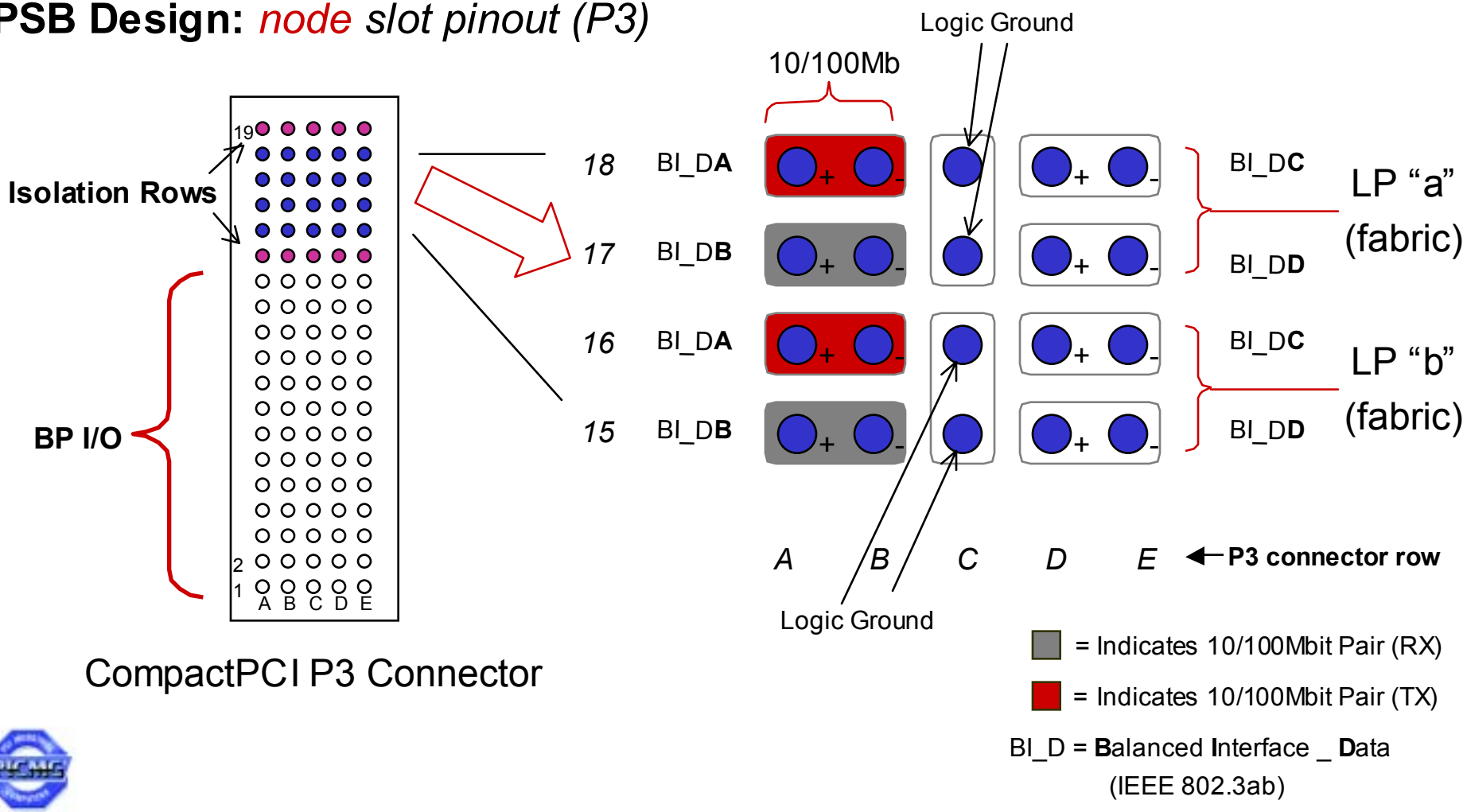
CompactPCI P1-P5 Backplane Connectors

Modified, CompactPCI/PSB uses ***ONLY*** 30 pins, 16 pins are active "link" connections, balance are ground and isolation pins.



How is it implemented?

PSB Design: *node slot pinout (P3)*

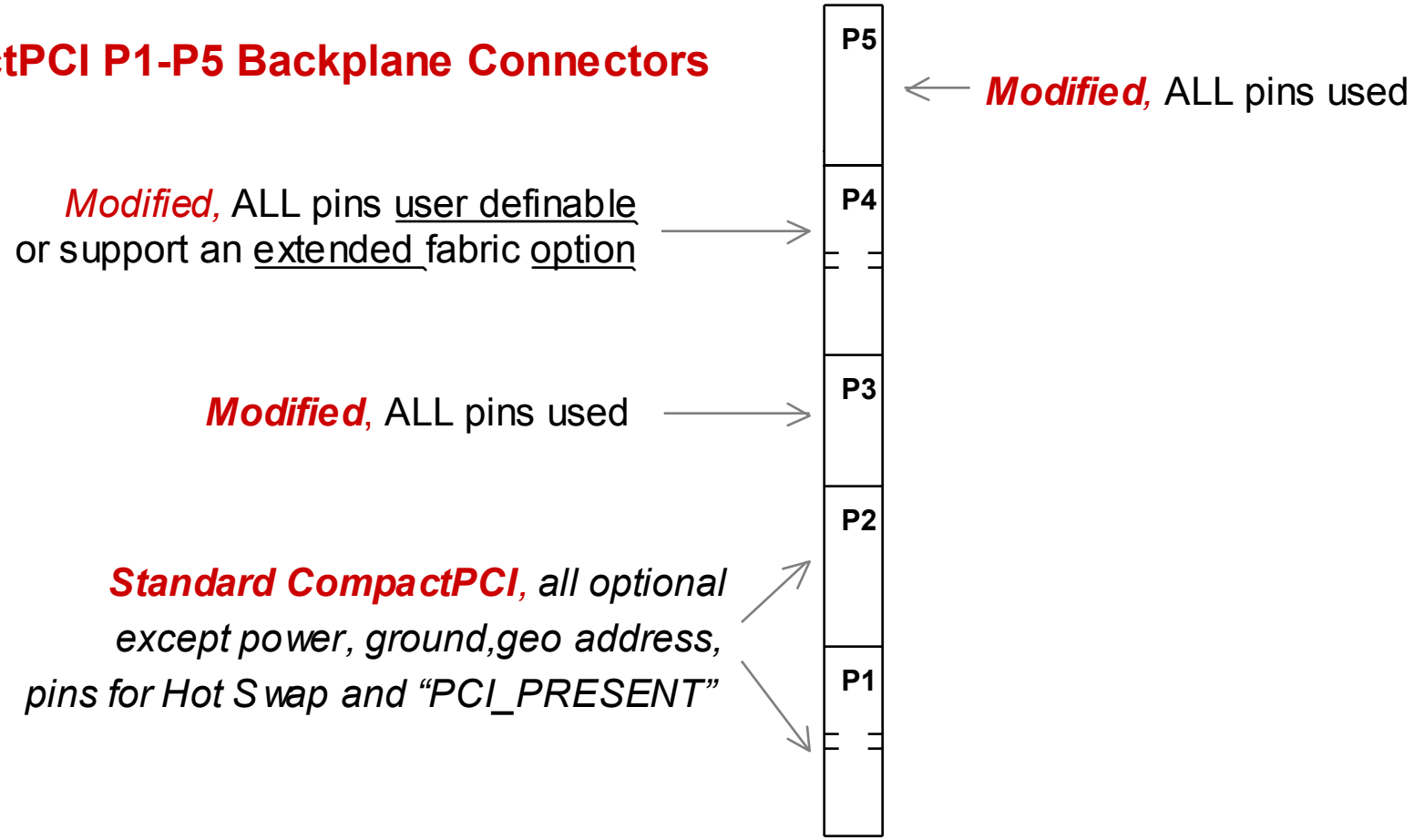


CompactPCI P3 Connector

How is it implemented?

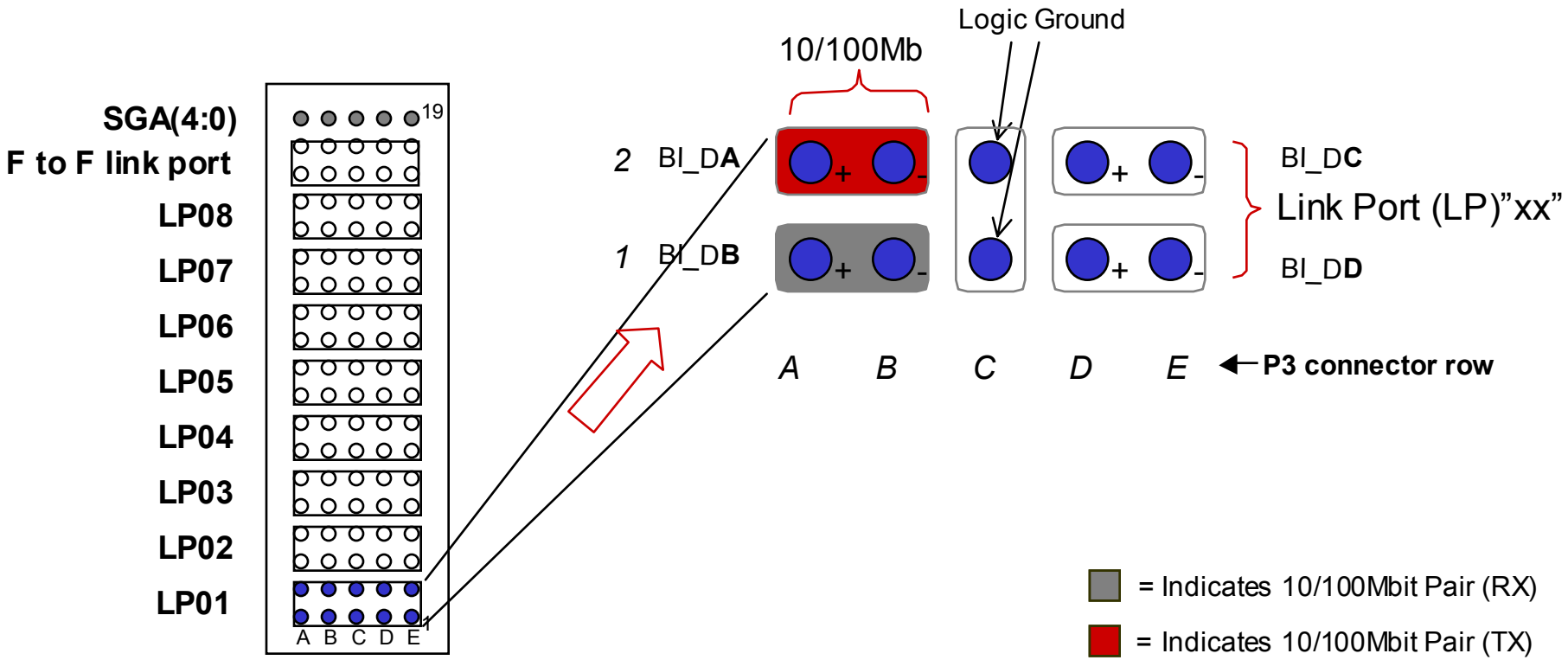
PSB Design: fabric slot connectors

CompactPCI P1-P5 Backplane Connectors



How is it implemented?

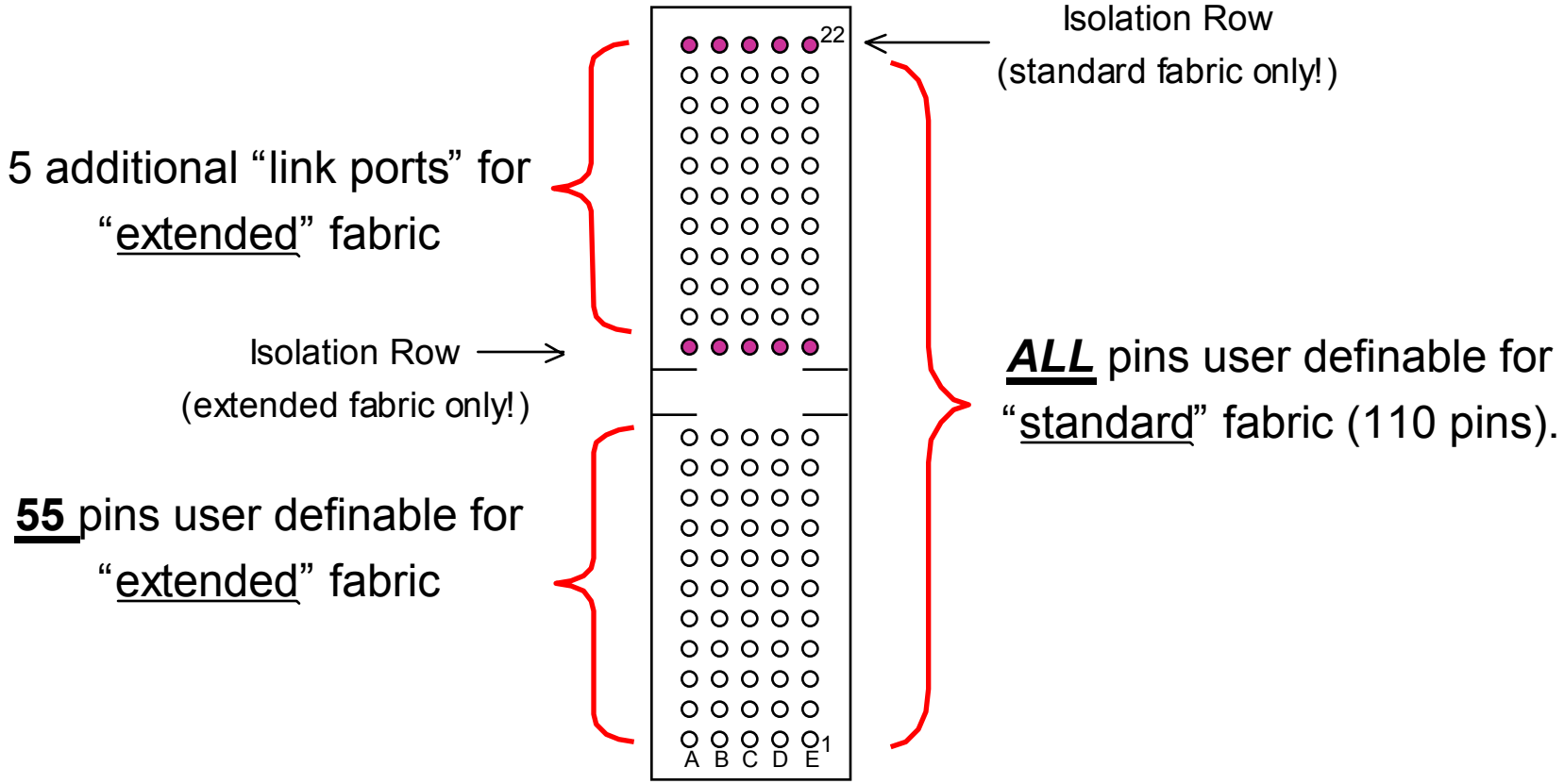
PSB Design: *fabric slot pinout (P3)*



CompactPCI P3 Connector

How is it implemented?

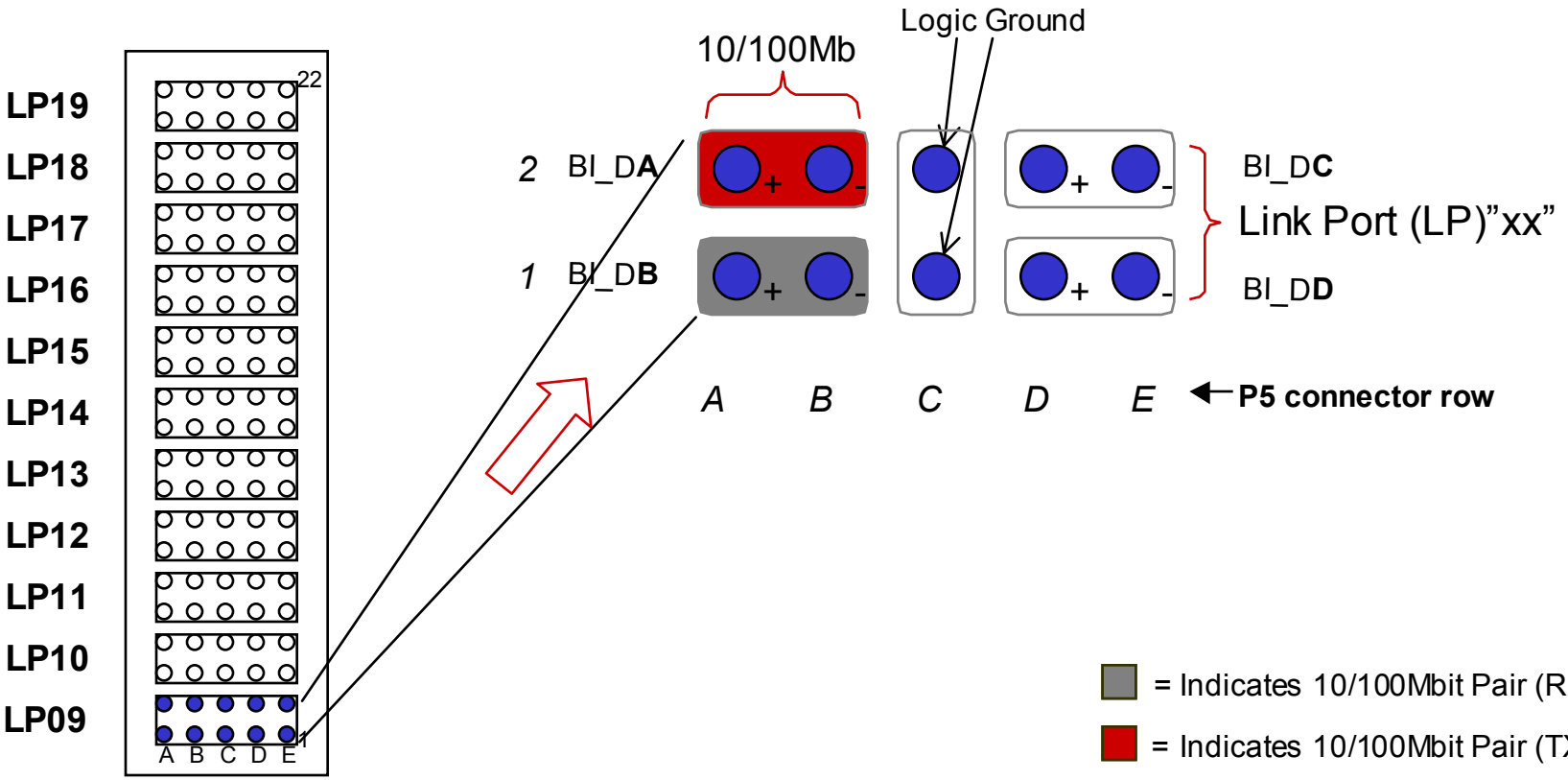
PSB Design: *fabric slot pinout (P4)*



CompactPCI P4 Connector

How is it implemented?

PSB Design: *fabric slot pinout (P5)*



CompactPCI P5 Connector

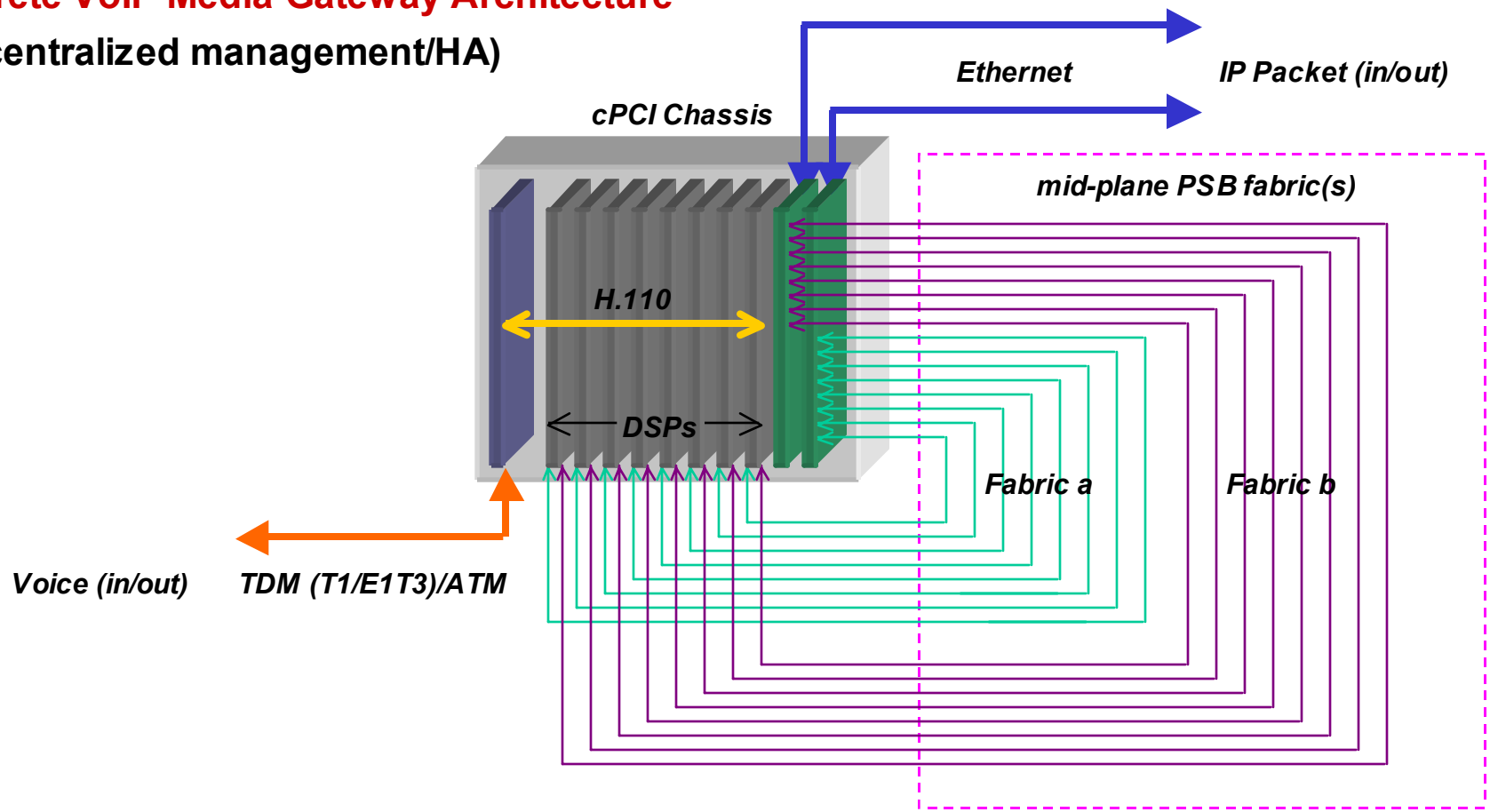
Some typical applications

- Voice over IP (VoIP) Media Gateways
- 2.5G and 3G Wireless Base Stations
- NG Cable Modems Headends
- Integrated Access Devices (IADs)
- IP Digital Subscriber Loop Access Multiplexors (DSLAMs)
- Embedded Server Clustering
- Integrated Video/Voice/Data Servers

Some typical applications

Discrete VoIP Media Gateway Architecture

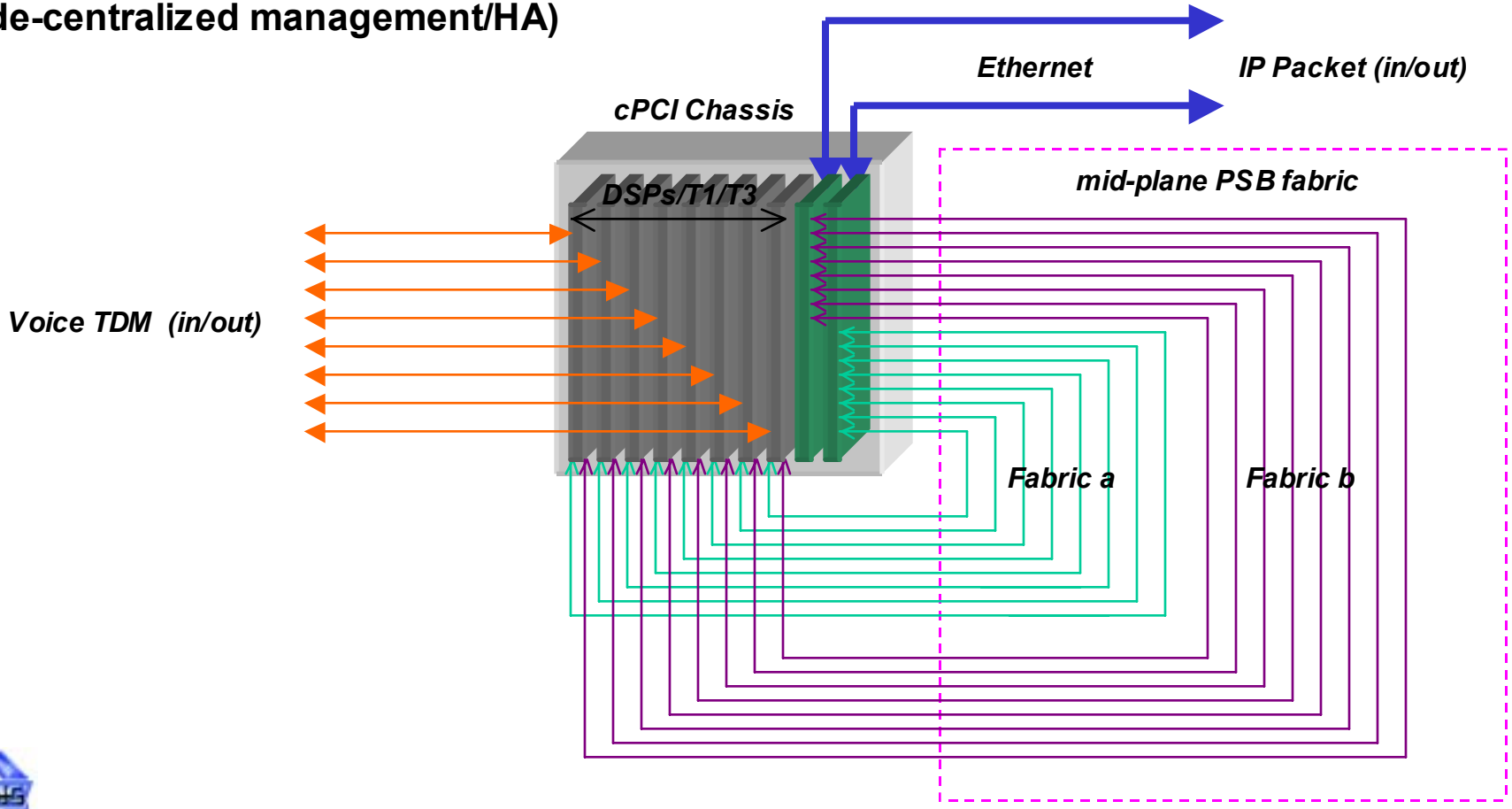
(de-centralized management/HA)



Some typical applications

Integrated VoIP Media Gateway Architecture

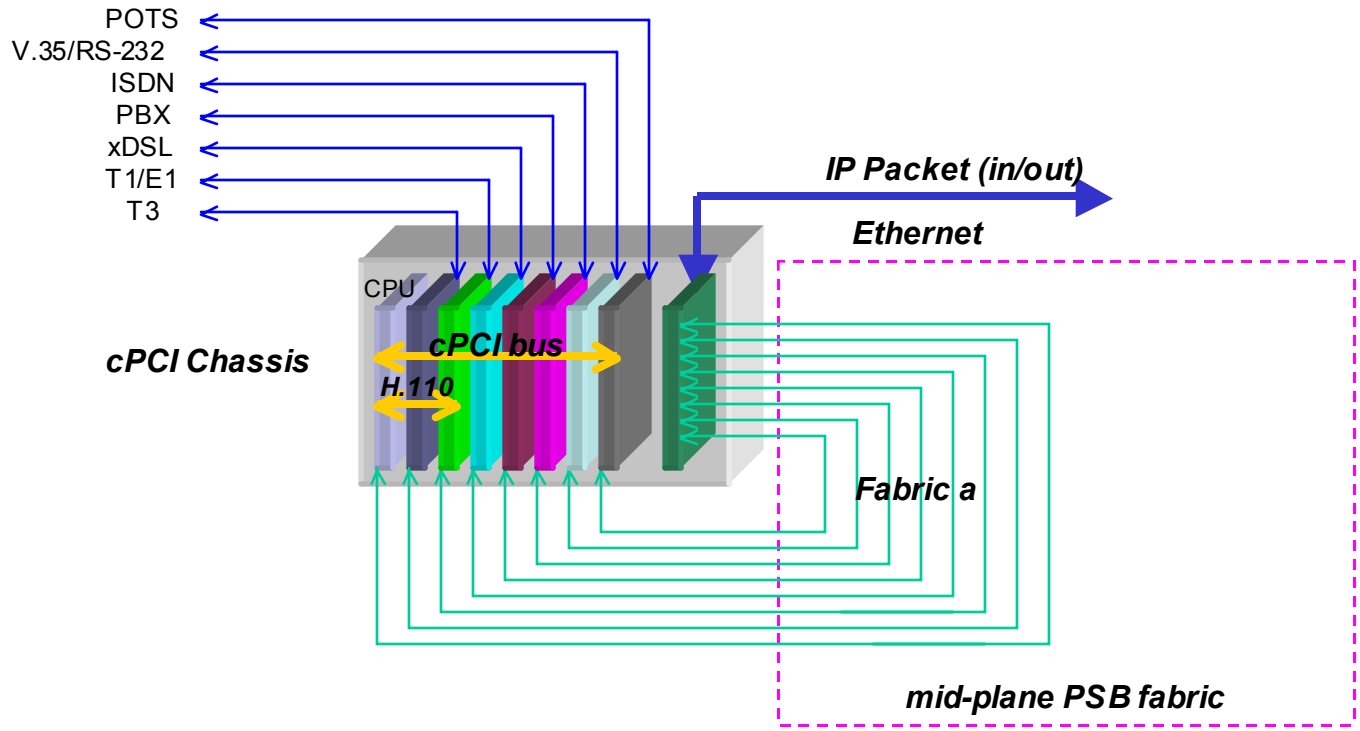
(de-centralized management/HA)



Some typical applications

Integrated Access Devices (IAD)

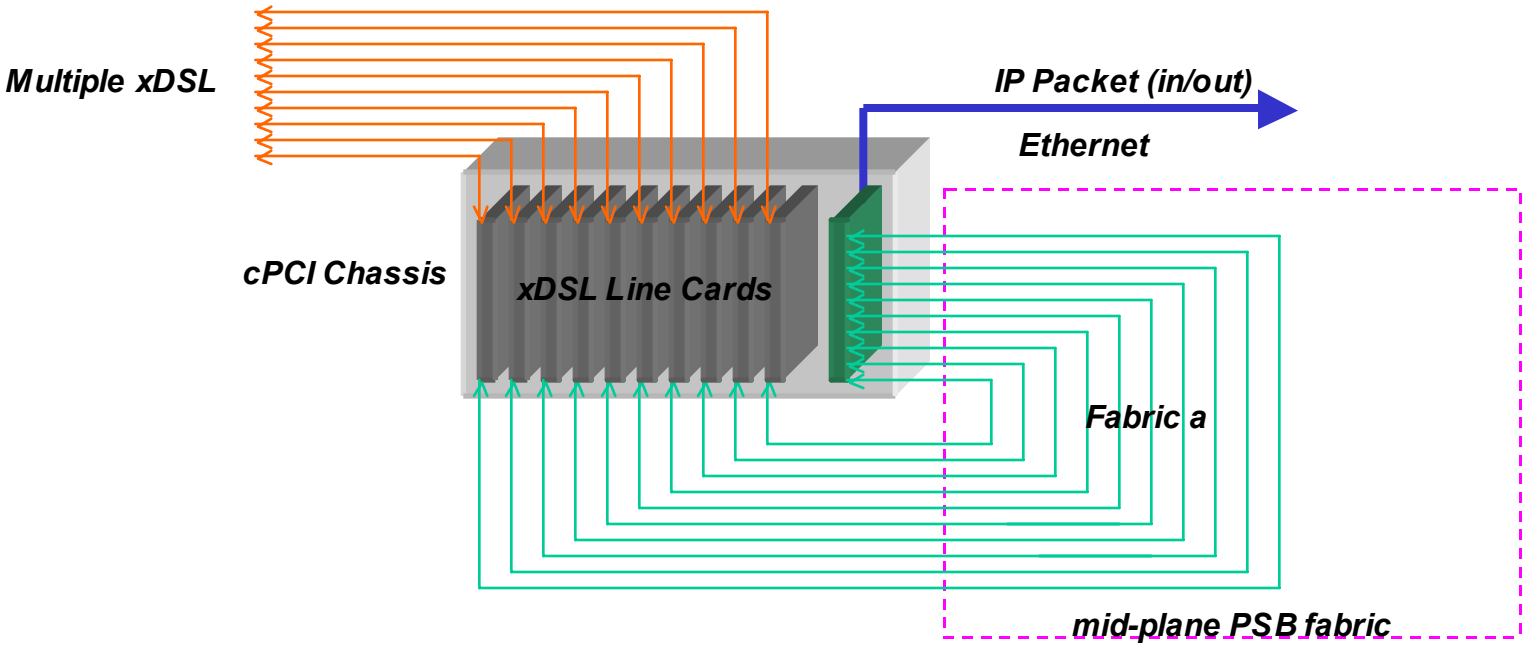
(centralized management/non-HA)



Some typical applications

IP DSLAM Architecture

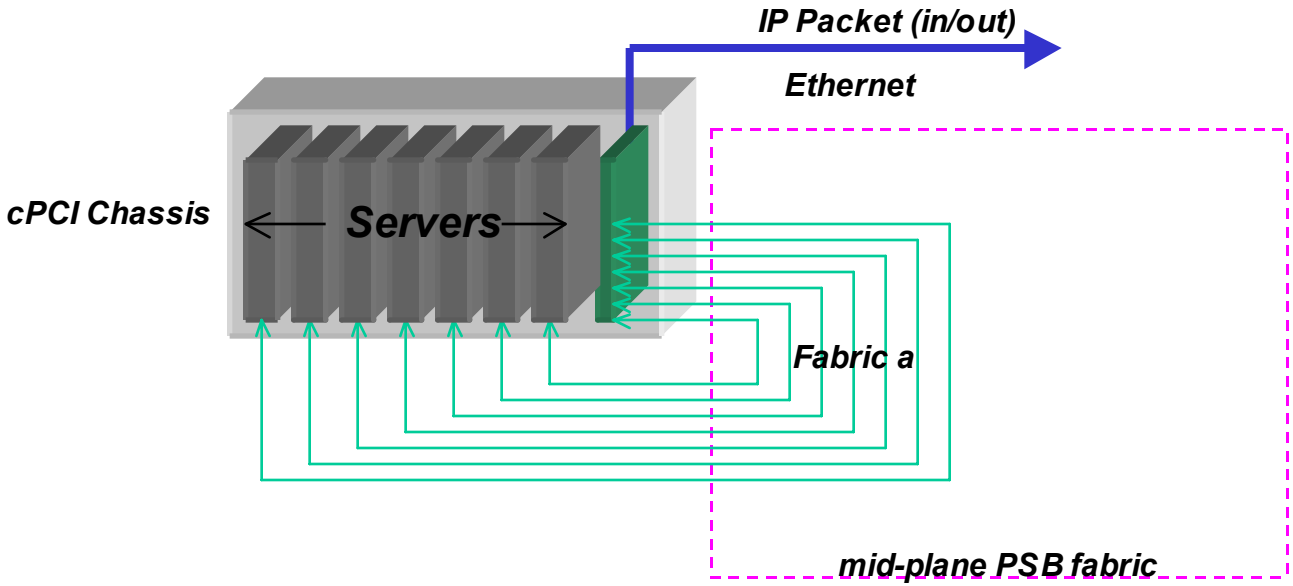
(de-centralized management/non-HA)



Some typical applications

Server Clustering Architecture

(de-centralized management/non-HA)



Summary

- Largest and fasting moving sub-committee in PICMG history.
- PICMG 2.16 on track to be finished in less than 10 months.
- 1st Packet Switching Architecture to be widely and quickly deployed.
- 1st Standards based backplane switching architecture to reach production.
- Fully redundant and capable of high chassis densities at initial deployment.
- Built on top of already existing standards and technology for *very* fast TTM.
- Leveraging of enterprise network industry ensures high volume IC market.
- Leveraging of enterprise networking protocols ensures SW interoperability.
- Embedded System Area Network architecture to significantly reduce TTM.
- Wide variety of products to be available the day the spec is ratified.
- Next generation PICMG 2.16 Packet Switching Backplane already started.

Q + A

Questions?